A Tunable SC Bandpass Delta-Sigma Modulator for Multi-Standard Applications

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Abstract—This paper presents a double-sampling switched-capacitor (SC) tunable resonator for bandpass (BP) ΔΣ modulators. The resonator is implemented with a single opamp to reduce the power consumption. In addition, the resonant frequency can be easily tuned by controlling the number of shunting capacitors. Based on the resonator, a fourth-order BP ΔΣ modulator is proposed. With the tuning ability, the resonant frequencies of the two resonators in the modulator not only can be varied to the same center frequency for narrow-band applications, but also to the frequencies symmetric to the center frequency, one quarter of the sampling frequency, for wide-band applications. The BP ΔΣ modulator is implemented in a 0.18μm CMOS technology, and Matlab and HSPICE simulation results are presented to demonstrate the design concept.

I. INTRODUCTION

BP ΔΣ modulators are very suitable to perform analog-to-digital conversion for IF signals due to its power efficiency compared to Nyquist-rate ADCs. Early work on BP ΔΣ modulators focused on narrow-band applications, and the center frequency was set to one quarter of the sampling frequency [1]-[3]. However, it is not practical for a multi-standard RF/IF receiver, which requires the modulator to be tunable and flexible. Tunable BP ΔΣ modulators using continuous-time loop filters have been reported [4][5]. Although continuous-time approach is more suitable for high-speed operation, it is difficult to control the center frequency, and the tuning methods are much more complicated than those of the SC counterparts. A tunable BP ΔΣ modulator proposed in [6] uses switched-capacitor delay cell to implement the resonator [1]. However, it requires two opamps for each resonator. The tunable double-sampling SC resonator proposed in [7] is realized by one opamp to reduce the power dissipation, but the circuit given in the paper cannot achieve the desired function. In this paper, we have modified the resonator circuit given in [7] to implement the desired tunable resonator function. In addition, the resonant frequency can be easily tuned by controlling the number of shunting capacitors. This resonator is then used to build a novel fourth-order BP ΔΣ modulator for multi-standard applications.

This paper is organized as follows. In Section II, a tunable SC resonator is described. A fourth-order tunable BP ΔΣ modulator realized by the resonator is discussed in Section III. In Section IV, the circuit implementation and the simulation results are presented.

II. PROPOSED TUNABLE RESONATOR

The transfer function of a tunable resonator is given by [8]

\[ H(z) = \frac{\alpha z^{-1}z^{-2}}{1-2\alpha z^{-1}+z^{-2}} \]  

(1)

where the resonant frequency is at

\[ f_o = \frac{\cos^{-1} \alpha}{2\pi} f_s. \]  

(2)

\( f_s \) is the sampling frequency. Note that \( f_o \) is located at \( f_s/4 \) for \( \alpha=0 \), and is at frequencies lower than \( f_s/4 \) for \( 0 < \alpha \leq 1 \) and is between \( f_s/4 \) and \( f_s/2 \) for \(-1 \leq \alpha < 0 \). Fig. 1 shows the possible block diagram of the resonator based on IIR transposed direct form II implementation [9]. One can see that two delay cells are needed for a resonator. As mentioned previously, it may require two opamps to realize the resonator. A double-sampling SC-resonator (\( \alpha=0 \)) using one single opamp has been proposed to reduce the opamp number, where

![Figure 1. Possible Block diagram of a resonator](image-url)
capacitors are used as the delay cell at the expense of complex clock phases [3]. Based on the circuits given in [3] and [7], a tunable double-sampling SC resonator is proposed as shown in Fig. 2, where the tuning factor \( \alpha \) is implemented by switching the shunting capacitors. The control signal \( S \) is set to high for positive \( \alpha \), and low for negative \( \alpha \). The clock waveforms are given in Fig. 3. The clock with subscript \( a \) (e.g. \( \phi a \)) denotes the clock slightly advanced with respect to the clock without subscript \( a \) (\( \phi \)). The output equations of the resonator (\( S \): high) in discrete-time domain during different clock phases are written as follows, where the corresponding phases are \( \phi 2o, \phi 1e, \phi 2e \) and \( \phi 1o \), respectively.

\[
\begin{align*}
C_{\phi a}V_{\text{OUT}}(n-3) &= C_{\phi a}V_{\text{OUT}}(n-5) + 2\alpha C_{f2}V_{\text{OUT}}(n-4) + C_{S2+}V_{\text{INV}}(n-5) + \alpha C_{12+}V_{\text{INV}}(n-4) \\
C_{\phi a}V_{\text{OUT}}(n-2) &= C_{\phi a}V_{\text{OUT}}(n-4) + 2\alpha C_{f1}V_{\text{OUT}}(n-3) + C_{S3+}V_{\text{INV}}(n-4) + \alpha C_{13+}V_{\text{INV}}(n-3) \\
C_{\phi a}V_{\text{OUT}}(n-1) &= C_{\phi a}V_{\text{OUT}}(n-3) + 2\alpha C_{f3}V_{\text{OUT}}(n-2) + C_{S4+}V_{\text{INV}}(n-3) + \alpha C_{14+}V_{\text{INV}}(n-2) \\
C_{\phi a}V_{\text{OUT}}(n) &= C_{\phi a}V_{\text{OUT}}(n-2) + 2\alpha C_{f4}V_{\text{OUT}}(n-1) + C_{S1+}V_{\text{INV}}(n-2) + \alpha C_{11+}V_{\text{INV}}(n-1)
\end{align*}
\]  

(3)

Assuming all the capacitances are matched and the signals are fully balanced, one can write the z-domain transfer function as given in (1).

III. FOURTH-ORDER TUNABLE BP \( \Delta \Sigma \) MODULATOR

A tunable fourth-order BP \( \Delta \Sigma \) Modulator can be implemented using the proposed resonator as shown in Fig. 4, where a low-distortion architecture [10] is employed with the integrators replaced by resonators [11][12]. \( b1 \) and \( b2 \) are the scaling factors. \( \alpha \) and \( \beta \) are tuning parameters for the first and second stages, respectively. For narrow-band cases, the two parameters can be set the same. Different from the previously reported approaches, the resonant frequencies are set differently to increase the SNDR for wideband applications. For example, one may place the two resonant frequencies of the fourth-order BP \( \Delta \Sigma \) modulator symmetric with respect to the center frequency. According to (2), the two resonant frequencies can be tuned by the same parameters but different in sign (\( \alpha = -\beta \)) if the center frequency is chosen as \( f_s/4 \).

Based on the result obtained in [13], the optimum zero locations for the 2nd-order lowpass delta-sigma modulator are \( \pm 1/\sqrt{3} \) of the bandwidth. For the bandpass case, the notch

Figure 3. Clocks of the resonator

Figure 4. Proposed fourth-order tunable BP \( \Delta \Sigma \) modulator
frequencies are

\[ \frac{f_s}{4} = \frac{1}{2\sqrt{3}} \frac{1}{f_B} \]  

(4)

where \( f_B \) is the bandwidth. One can then find the optimum value for \( \alpha \) as the following equation.

\[ \alpha = -\beta = \sin\left(\frac{\pi}{2\sqrt{3}\text{OSR}}\right) \]  

(5)

IV. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

The tunable fourth-order BP ΔΣ Modulator with one-bit quantizer is implemented in a 0.18\( \mu \)m CMOS technology. The supply voltage is 1.5V and the power consumption is 22mW. The differential reference voltages are 1.2 and 0.3V, respectively (common-mode voltage of 0.75V). The tuning parameters are controlled by a 4-bit word, and the step is 0.0625. The layout of the core is shown in Fig. 5, where the area is 0.68\( \times \)0.5 mm\(^2\) and the total area including pads is about 1.09\( \times \)0.9 mm\(^2\). The modulator has been simulated using HSPICE. The first example is a wideband case, where the sampling frequency and the center frequency are 80 MHz and 20 MHz, respectively. The bandwidth is 5MHz, and the resulting OSR is 8. According to (5), the optimum value for \( \alpha \) and \( \beta \) is 0.113 and -0.113, respectively. Due to the finite resolution of the tuning capacitors, \( \pm 0.125 \) is used. Fig. 6 shows the output spectra of the modulator with the scaling parameters \( b1 = b2 = 0.5 \), and -6 dBFS input. The FFT was calculated from 8192 samples applied with Hanning window. The resulting SNDR is about 26dB. Fig. 7 shows the SNDR with respect to the input level, where the peak SNDR is 28dB. Capacitor mismatch is also taken into account. For a standard deviation of mismatch error of 0.5%, the mean and the standard deviation of SNDRs obtained from 1000 MATLAB simulation samples are 24.3dB and 1.27dB, respectively.

Another example with \( \alpha = -\beta = 0.1875 \) is given in Fig. 8.
For the center frequency different from $f_c/4$, one may adjust the tuning parameters to achieve the desired noise shaping. Fig. 9 (a) and (b) show the output spectra of the tunable modulator with $\alpha = \beta = 0.125$ and $-0.125$, respectively. The corresponding SNDRs are 46.3dB and 51.4dB for OSR=32 and -6 dBFS input.

V. CONCLUSION

A double-sampling tunable SC resonator for BP $\Delta\Sigma$ modulators is presented. The resonator is implemented with a single opamp to reduce the power consumption. A novel fourth-order BP $\Delta\Sigma$ modulator is implemented using the proposed resonator. The tuning feature provides the flexibility to adjust the modulator to the desired center frequency and also to minimize the SNDR for different communication standards. Although, only one-bit quantizer is used in this design, it can be easily expanded to a multi-bit output to achieve the desired performance. In addition, the BP $\Delta\Sigma$ modulator can be used in the lowpass case by proper scaling. The modulator has been fabricated in a 0.18μm CMOS technology, and the measurement results will be reported later.

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