Design of The Low Voltage Concurrent Dual-Band CMOS LNA
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Abstract
In this paper we employ TSMC CMOS 0.25 um process to design a concurrent dual band low noise amplifier (LNA) on low voltage work. We use a folded cascode LNA to reduce the supply voltage. We folded the second stage common gate transistor of the general cascode to another biasing path, therefore the supply voltage just has to bias one transistor in each biasing path. Consider the RF condition, we use a capacitor to couple the RF signal between the two biasing path and make circuit work like a tradition cascode LNA at RF. In addition, we design a concurrent dual band LNA employ one parallel LC tank. Due to this LNA not need independence two received paths and not need switch to change receive path like tradition dual band LNA, so it can save the design area.

1. Introduction
Recently, dual-band transceivers have been introduced to increase the functionality of such communication systems by switching between two different bands to receive one band at a time. However, simultaneous operation at different frequency bands can only be achieved by building multiple independent signal paths with an inevitable increase in the footprint, power dissipation and cost. In this paper, concurrent dual-band receiver architecture is introduced that is able to simultaneous operation at two different frequencies without dissipating twice as much power or a significant increase in footprint and cost. The concurrent multiband LNA in the concurrent dual-band receiver proposed provide simultaneous narrow-band input matching and gain at multiple frequency bands, while maintaining low noise.

In this paper, the complete circuit is simulated by Agilent Advanced Design System (ADS), and will be fabricated in TSMC 0.25 µm CMOS process.

2. LNA Design
The first component of wireless communication receiver is typically a low noise amplifier (LNA). Its main role is to provide enough gain to overcome the noise of subsequent stages. An LNA not only providing this gain while adding as little noise as possible, but also should accommodate large signals without distortion, and frequently must also present a specific impedance, such as 50 Ω, to the input source. In order to get better linearity and noise performance, we should make the noise figure and distortion as small as possible in LNA part to meet the receiver sensitivity.

LNA amplifies the weak signal from the antenna/duplex filter with contributing small noise to the next stage by introducing inherent noise as low as possible. Therefore, if the CMOS technology is to be used in demanding applications, it is important to be able to design CMOS LNA with very low noise. The requirement of LNA is low noise, high linearity, sufficiently high gain, well-defined resistive input impedance, and low power consumption, respectively.

In this section, we will introduce the noise analysis of MOS transistor and overview the basic configurations of LNA. In addition, we will discuss the relation of noise matching and power watching.

The main noise sources of MOSFET are the thermal noise of the drain noise $i_{nd}^2$, gate noise $v_{ng}^2$ and source resistance noise $i_{rs}^2$, so we will discuss in this section. The noise model of MOSFET is shown Fig. 1.

From the Fig. 1, the source resistor noise current can be to regarded as source resistor series a noise voltage source $v_{ns}^2$, and the noise source equation can be expressed as following:

$$v_{ng}^2 = 4kT R_g \Delta f$$  \hspace{1cm} (1)

$$v_{ns}^2 = 4kT R_s \Delta f$$  \hspace{1cm} (2)

$$i_{nd}^2 = 4kT g_{ds} \Delta f \approx 4kT g_{m}^\gamma \Delta f$$  \hspace{1cm} (3)

where, $k$ is the Boltzman constant, $T$ is the absolute temperature, $\Delta f$ is the noise bandwidth, $\gamma$ is a bias dependent parameter, $g_{ds}$ is drain-source conductance at zero $V_{DS}$ which is typically equal to $g_{m}$, because the $\alpha = g_m / g_{ds}$ and $\alpha$ is unity for long-channel devices and progressively decreases as channel lengths shrink, it is one measure of the departure from the long-channel regime. For long-channel devices, the value is

$$\frac{2}{3} < \gamma < 1$$  \hspace{1cm} (4)

Unfortunately, measurements show that short-channel devices in saturation exhibit noise far in excess of values predicted by long-channel theory, sometimes by large factors ($\gamma$ is typically 2-3, but can be considerably larger).

In addition, a common noise shape is that of 1/f, or flicker noise. In the carrier-density fluctuating model, the noise is explained by the fluctuating of the channel free carriers due to the random capture and emission...
by the interface traps known as slow states. The spectral density, $V_n^2(f)$, of 1/f noise is approximated by

$$V_n^2(f) = \frac{k_v^2}{f}$$

(5)

where $k_v$ is a constant. Thus, the spectral density is inversely proportional to frequency.

Note that, because the LNA is operated in high frequency, therefore this flicker noise source usually small enough to be neglected.

The design methods of LNA mainly have two types of topologies, one for noise matching and other for power matching. Thereinafter we will discuss them.

In LNA design, we use low noise match for input matching network and use conjugate match for output matching network to obtain the best noise performance. We employ a common source amplifier to get an example.

One straightforward approach to providing a reasonably broadband $\Omega = 50\Omega$ termination is simply to put a $\Omega = 50\Omega$ resistor across the input terminals of a common source amplifier, as shown in Fig. 2.

Unfortunately, the resistor $R_1$ adds thermal noise of its own, and attenuates the signal to the transistor. These effects generally produce unacceptably high noise figures. We can establish the following lower bound on the noise figure of this circuit with $R_{so} = R_1 = R$:

$$F \geq 2 + \frac{4\gamma}{\alpha} \frac{1}{g_n R}$$

(6)

This bound applies only in the low frequency limit and ignores gate current noise. Naturally, the noise figure is worse at higher frequencies and when gate noise is taken into account.

The noise figure of a two-port amplifier is presented in equation 7.

$$F = F_{min} + \frac{R_n}{g_s} \left| y_s - y_{opt} \right|^2$$

(7)

In equation 7, $R_n$ is equivalent noise resistance of transistor, $g_s$ is real part of source admittance, $y_s = g_s + j\beta_s$ represents the normalized source admittance, $y_{opt}$ represents optimum source admittance that results in minimum noise figure, $F_{min}$ is minimum noise figure of transistor, we can obtained when $y_s = y_{opt}$. The $y_s$ and $y_{opt}$ can be expressed in term of the reflection coefficients $\Gamma_s$ and $\Gamma_{opt}$ as

$$y_s = \frac{1}{Z_0} \frac{1 - \Gamma_s}{1 + \Gamma_s}$$

(8)

$$y_{opt} = \frac{1}{Z_0} \frac{1 - \Gamma_{opt}}{1 + \Gamma_{opt}}$$

(9)

Therefore,

$$\left| y_s - y_{opt} \right|^2 = \frac{4}{Z_0^2} \left| \frac{\Gamma_s - \Gamma_{opt}}{1 + \Gamma_s} \right|^2$$

(10)

$$g_s = \text{Re}(y_s) = \frac{1}{2Z_0} \left( \frac{1 - \Gamma_s}{1 + \Gamma_s} + \frac{1 - \Gamma_{opt}}{1 + \Gamma_{opt}} \right) = \frac{1}{Z_0} \left( \frac{1 - \Gamma_s^2}{1 + \Gamma_s^2} \right)$$

(11)

Using these results, equation 7 can be written as following:

$$F = F_{min} + \frac{4R_n}{g_s} \left| \frac{\Gamma_s - \Gamma_{opt}}{1 + \Gamma_s} \right|^2$$

(12)

We must have a small noise figure and sufficient power gain, when we design a LNA. If we want contain a minimum noise figure and maximum power gain, simultaneously, we must set $S_{11}^* = \Gamma_{opt}$. Unfortunately, this condition is not easy to reach. Usually, this is a tradeoff condition. We have a feasible manner by using source series feedback skill (Fig. 3). Of course the gain must be decreased, but the $S_{11}^*$ and $\Gamma_{opt}$ would be close to each other.

3. Low voltage Topology

A lot of LNA designs use cascode topology, although cascode topology has many advantages, but it has two transistors in the biasing rail. It is not suitable for low supply voltage design. In Fig. 4, we have illustrated the low-voltage topology scheme. The proposed scheme uses two on-chip LC tanks and one coupling capacitor. The LC tank is to provide low impedance at dc and relatively high impedances at RF.

The coupling capacitor is to couple the RF signals between the two elements. In this architecture, there is no dc current shared between the two elements because of the coupling capacitor. Furthermore, the LC tanks require no dc voltage headroom, the minimum voltage supply required is only $V_{th}$. The LC tanks essentially become open circuits at RF and the coupling capacitor couples the RF signal between the two elements. We will use this topology to improve the typically cascode LNA for low voltage design.

4. Concurrent Dual-Band Topology

Now, we will introduce concurrent dual-band receiver architecture. It is capable of simultaneous operation at two different frequencies without dissipating twice as much power or a significant increase in cost and footprint. Fig. 5 shows the conceptual evolution of a dual-band receiver, starting
with two totally independent receive paths, and leading to an efficient concurrent dual-band receiver. Due to the concurrent dual-band receiver can simultaneous receive at both bands, so it does not need any switch or diplexer. The first gain stage is LNA, it provides simultaneous gain and matching at two bands. Fig. 6 is a concurrent dual-band LNA architecture. In the input, there is a parallel LC network. The resonant frequency of this parallel LC network is tuned between the desired two bands. The parallel LC network function is similar band-reject filter. It can increase sensitivity of this concurrent dual-band LNA. The drain load network should exhibit high impedance only at frequencies of interest in order to achieve concurrent dual-band gain. This requirement can be fulfilled by add a series LC branch in parallel with the parallel LC tank of a single-band LNA, as shown in Fig. 6.

5. Proposed LNA Implementation and Layout

Fig. 7 shows the proposed concurrent dual-band low voltage folded cascode LNA. MOSFET M2 is used to reduce the interaction of the tuned output with the tuned input, and to reduce the effect of M1’s $C_{gd}$. The MOSFET M3 essentially forms a current mirror with M1, and its width is some small fraction of M1’s width to minimize the power overhead of the bias circuit. The supply voltage and $R_{ref}$ in conjunction with $V_{gs}$ of M3 can set the M3 current through. The resistor $R_{bias}$ is chosen large enough that its equivalent noise current is small enough to be ignored. The DC blocking capacitor Cb must be presented to prevent upsetting the gate-to-source bias of M1, the value of Cb is chosen to have a negligible reactance at the signal frequency, and it sometimes implemented an off-chip component, depending on the value required and die area constraints. In the output stage, we use a MOSFET M4 and a resistor Rt to improve output match. This stage is a common drain topology, we can employ Rt to control M4 current through. On the other hand, we can rely on change the M4 current to adjust M4’s transconductance. Therefore, the output match can be complete. The summary performances of this circuit is shown in Table 1.

Fig. 8 is the layout circuit. (0.965 × 0.946 mm$^2$).

6. Conclusion

In this paper, we design a concurrent dual-band LNA operation in low-voltage. The RF input signals are 2.4GHz and 5.2GHz, respectively. It is operating at supply voltage of 1.2V and in TSMC 0.25 um CMOS process. The circuit is simulated using Agilent Advanced design system (ADS). The summary performances of this circuit are shown in Table 1, and the measurement result will be reported later.

7. References

Fig. 2 Common source amplifier with shunt input resistor

Fig. 3 Series feedback skill

Fig. 4 Low voltage topology

Fig. 5 Concurrent dual-band receiver

Fig. 6 Concurrent dual-band LNA

Fig. 7 Proposed concurrent dual-band folded casode LNA

Table 1 Summary of the LNA performances

<table>
<thead>
<tr>
<th>Frequency Range</th>
<th>2.4GHz</th>
<th>5.2GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2V</td>
<td>1.2V</td>
</tr>
<tr>
<td>Input Return Loss (dB)</td>
<td>-20.696</td>
<td>-16.098</td>
</tr>
<tr>
<td>Output Return Loss (dB)</td>
<td>-19.842</td>
<td>-24.645</td>
</tr>
<tr>
<td>Reverse Isolation (dB)</td>
<td>-56.846</td>
<td>-41.957</td>
</tr>
<tr>
<td>Power Gain (dB)</td>
<td>11.715</td>
<td>9.826</td>
</tr>
<tr>
<td>Noise Figure (dB)</td>
<td>3.020</td>
<td>4.608</td>
</tr>
<tr>
<td>NFmin (dBm)</td>
<td>-12.726</td>
<td>-12.529</td>
</tr>
<tr>
<td>NFmax (dBm)</td>
<td>-1.909</td>
<td>-1.227</td>
</tr>
<tr>
<td>IP3 (dBm)</td>
<td>14.904</td>
<td></td>
</tr>
<tr>
<td>DC Current (mA)</td>
<td>33</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 8 Circuit layout